# Trilinear

# DisplayPort Receiver

Our 6th generation DisplayPort Receiver Link Controller core supports DisplayPort 2.1, DisplayPort 1.4a and embedded DisplayPort 1.5.

Features include link rates up to 20Gbps for DisplayPort 2.0, 8.1Gbps for DisplayPort 1.4a. Display Steam Compression (DSC), multi-stream transport (MST) and more. The base core includes all required link functionality— Main Link, Secondary Channel, and AUX Channel protocols—and supports the HDCP 2.3 standards for data encryption.

The DisplayPort Receiver core interfaces use common industry standards for low-complexity integration.

# AT A GLANCE:

- Silicon proven on multiple ASIC and FPGA processes with multiple PHY partners
- 1, 2 or 4 pixels per input cycle, supporting up to 16K resolution input per source
- 1.62-20Gbps (8.1Gbps max for 1.4a)
  link rate across 1, 2, 3, or 4 lanes
- SST or MST operation
- Full secondary channel support
- Real time HDCP 1.4/2.3 support
- Optional eDP 1.5 support including enhanced Panel Replay Protocol
- Meets VESA Standard Compliance
- Deep color and HDR support up to 16 bits of color
- DSC transport with Forward Error Correction support
- Interfaces to external PHY.
  Compatible with 3rd-party PHYs for ASICs from 7nm to 65nm technologies; FPGA-targeted implementations are also available

#### Video In

Streaming interface with industry-standard flow control, including separate syncs and data enable. Frame and line delimiter signals are supported with either 1, 2 or 4 pixels per input clock cycle.

42-bit pixel inputs provide deep color support. Other color depths are chosen through selective use of these input ports.

#### Audio

Multi-port I2S interface with up to 32 audio channels for digital audio transport.

#### Host

32-bit AMBA Peripheral Bus (APB), 4 slave port for low-complexity transfers of configuration information to the core.

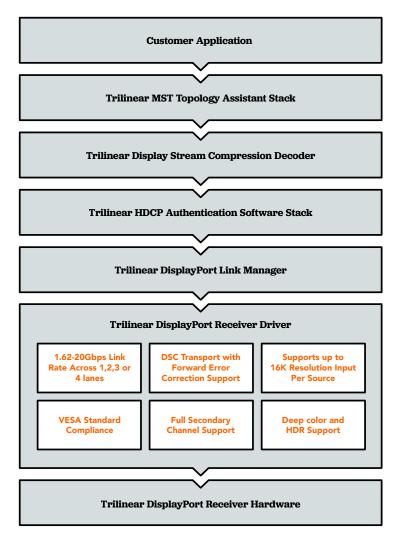


Figure 1. Trilinear DisplayPort Receiver Driver

TRILINEAR TECHNOLOGIES STANDING THE TEST — EVERY TEST, EVERY TIME.



### **Delivery & Availability**

The DisplayPort Receiver core ships with a DisplayPort-compliant link policy maker software stack and a fully documented API. The core is available as a soft core in one of several configurations, including off-the-shelf versions or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge. Trilinear also provides custom integration services for the delivery of a complete solution on each customer target technology.

The DisplayPort Receiver Link Controller core is also available on the Trilinear Technologies' Cobra Development Platform. This FPGAbased reference system provides a complete development environment for core evaluation as well as early software development.

## **Verification Testing**

Verification testing has been completed using a bottom-to-top methodology. Testing is first performed at the module level and progresses up to system level. With the DisplayPort Receiver, module-level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

Trilinear Technologies validated core compliance using the DisplayPort compliance test suite. The results of compliance testing are available upon request. Extensive interoperability testing included a wide range of shipping products.

The core ships with a self-checking test bench, intended to illustrate the proper management of the input and output interfaces.

# **Design Database**

Trilinear Technologies delivers an extensive design database for the HDMI Receiver core. The database includes all the files required to implement the design on multiple platforms, including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included, along with associated documentation to reduce the amount of time for software development.

#### Files and data include:

- HDL source files for the function design
- Fully functional models for block-level and top-level testing, including over 120+ tests in the user level environment
- Functional specification
- Timing constraints summary document
- IP-XACT register descriptions
- Generic SRAM simulation models
- C Reference Driver



