VF-117R DisplayPort Receiver Link Controller

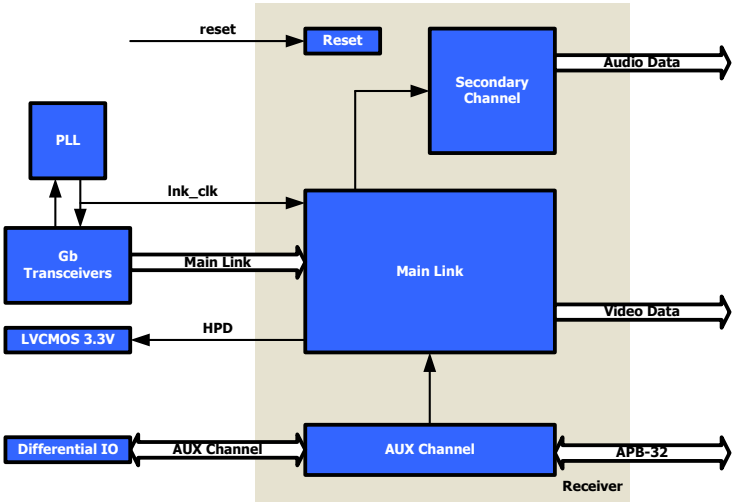
The Trilinear Technologies VF-117R Link Controller is a fifth-generation core which implements support for the DisplayPort 1.4 standard. The highly integrated design includes the Main Link, Secondary Channel and AUX Channel functions. In addition, HDCP and embedded DisplayPort support are available. The core is highly configurable and can support multiple link rates from 1.62Gbps to 8.1Gbps across 1, 2, or 4 lanes.

The Trilinear VF-117R core has been thoroughly validated using industry accepted DisplayPort compliance test suites. In addition, the core has passed significant interoperability testing and is shipping in numerous production systems. The core is currently shipping in both ASIC and FPGA implementations.

The video output port is implemented using an industry standard sync and data interface which simplifies integration into existing systems. For systems that include a host processor, access is provided via a 32-bit AMBA APB4 bus interface. For most receiver applications, a host processor is not required. Audio interfaces are supported through multiple I2S ports or a SPDIF port. An integrated I2C master provides access to either on-chip or an external EDID ROM.

The VF-117R core ships with a DisplayPort compliant software stack and a fully documented API. The core is available for evaluation on the Trilinear Technologies' Cobra Development platform. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- Implements DisplayPort 1.4
- Supports SST, MST, DSC 1.2 and FEC
- Embedded DisplayPort 1.4b
- Main link, secondary channel, HDCP 1.3, HDCP 2.2
- Capable of operating without a host CPU in low complexity applications.
- Silicon proven on multiple ASIC and FPGA processes

Interfaces

- Standard VS/HS video interface
- 1, 2 or 4 pixels per output cycle up to 8192 x 8192 output.
- AMBA APB4 Slave Interface
- I2S or SPDIF Audio Output

Core Details

- Multiple link rate support from 1.62Gbps to 8.1Gbps across 1,2, or 4 lanes
- Secondary channel support including audio and camera
- HDCP 1.3 and 2.2 support in SST and MST modes
- eDP 1.4b support
- Deep color and HDR support

Reference Software

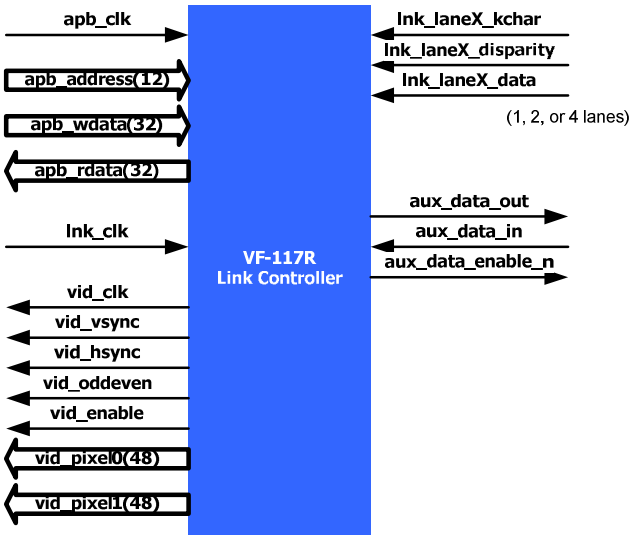
- Complete DisplayPort 1.4 device driver.
- Low complexity driver for systems requiring a host processor
- Sample core configuration
- Fully documented API

CORE INTERFACES

Host processor access is implemented as a 32-bit, AMBA APB4 Peripheral Bus (APB) slave interface. The APB provides low complexity transfers of configuration information to the core.

The VF-117R Link Controller core includes a standard streaming interface for output video. Using vertical and horizontal syncs, the output port provides both progressive and interlaced outputs. Timing accurate or DMA transfer modes are available.

Output image data is transferred via a streaming interface with industry standard flow control. Vertical and horizontal delimiter signals are supported with 1, 2, or 4 pixels per cycle. Deep color is supported using 48-bit pixel outputs. Other color depths are supported through selective use of these ports.



PHY INTERFACE

The Trilinear VF-117R Link Controller interfaces to an external PHY which implements the gigabit transceivers necessary for the DisplayPort 1.4 standard. The core implements a generic PHY interface that can be used to connect to a third party PHY. Several PHY implementations in both FPGA and ASIC platforms are currently available from Trilinear Technologies. Please contact a sales representative for more information.

VERIFICATION TESTING

Trilinear Technologies has validated the core using a robust DisplayPort compliance test suite. Testing includes a wide variety of standards compliance and interoperability testing. The results of compliance testing are available upon request. Extensive interoperability testing has also been conducted using a hardware prototype with a wide variety of shipping video sources.

RTL Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the VF-117R receiver core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

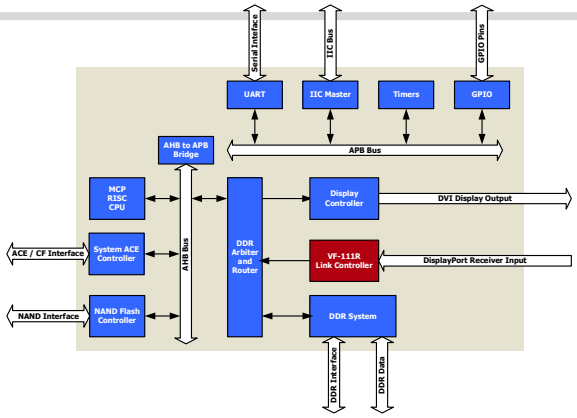
Trilinear Technologies delivers an extensive design database for the VF-117R receiver core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for basic core testing
- User's Guide
- Integrator's Guide
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver

REFERENCE HARDWARE

The VF-117R core is available for demonstration and early software prototyping on the Trilinear “Cobra” development system. The Cobra development system is based on the Xilinx kc705 board and provides a high degree of functionality including a 32-bit MIPS processor capable of running custom applications.

Using the integrated SD Card interface, custom application software can be loaded onto the system for early development. The video input system uses a daughter card for DisplayPort connectivity. Each Cobra system includes a host processor and peripheral suite running a flash based ROM monitor which loads at power up. The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The VF-117R Link Controller is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit RISC processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or SD Card storage system
- Includes traditional shell commands

DDR-3 Memory System

- 512 MB SODIMM
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard DVI Interface and LCD Controller

- Programmable display timing controller
- Display path supports multiple color depths
- HDMI Output up to 1900x1200 (154MHz)
- DisplayPort 1.4 output up to 4096 x 4096

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx kc705 Based System

- Xilinx Kintex-7 FPGA
- Secure Digital card mass storage
- DVI Output Port

VF-117R DisplayPort Receiver

- Triple speed, 4 lanes
- Daughter card connection
- DisplayPort to HDMI connection

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