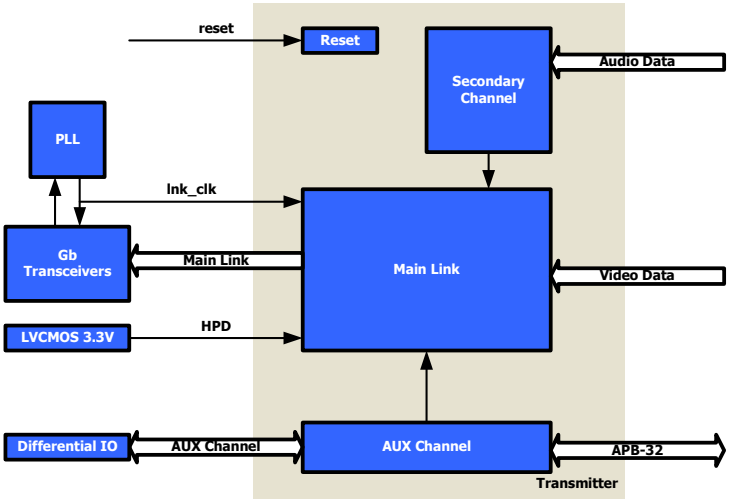
VF-111T DisplayPort Transmitter Link Controller

The VF-111T DisplayPort Transmitter core from Trilinear represents the fifth-generation link controller which includes support for DisplayPort 1.4 and embedded DisplayPort 1.4b features including link rates up to 8.1Gbps, Display Stream Compression (DSC 1.2), multi-stream transport (MST) and more. The base core includes all the required link functionality including Main Link, Secondary Channel and AUX Channel protocols. In addition, the core supports the HDCP 1.3 and HDCP 2.2 standards for data encryption.

The interfaces to the VF-111T core utilize common industry standards for low complexity integration. The primary video interface uses a simple VS/HS video interface which simplifies integration into existing systems. For the optional transport of digital audio information, the design implements a multi-port I2S interface supporting up to 8 channels of audio. The AMBA APB4 slave port provides a low complexity host interface which is compatible with most target systems with only a small amount of external glue logic required. Trilinear provides custom integration services for the delivery of a complete solution on each customer target technology.

The VF-111T core ships with a DisplayPort compliant link policy maker software stack and a fully documented API. The core is available on the Trilinear Technologies' Cobra Development platform. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- DisplayPort 1.4 support including HBR3 and MST.
- Embedded DisplayPort 1.4b
- Multiple process PHY support including 28nm, 40nm, and 65nm.
- DSC 1.2 with FEC supported
- Link policy maker SW included

Interfaces

- Standard VS/HS video interface
- 1, 2 or 4 pixels per input cycle
- 135MHz / 81MHz or 108MHz reference clock
- AMBA APB4 Slave Interface

Core Details

- Multiple link rate support across 1,2, or 4 lanes
- SST or MST operation
- Secondary channel support
- Optional HDCP 1.3/2.2 support
- Optional eDP 1.4b support
- Deep color and HDR support

Reference Software

- DisplayPort 1.4 compliant link policy maker
- 'C' source code included
- Fully documented API

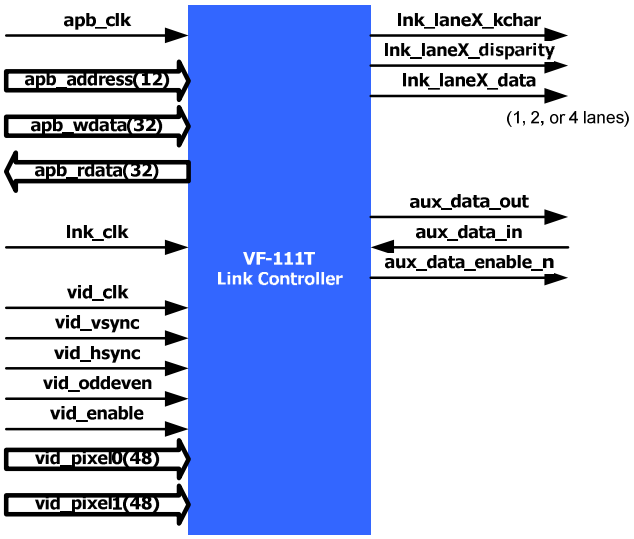
FPGA Development Platform

- 32-bit MCU based system
- Real time video input
- Includes the VF-111T Link Controller, DDR-3 system and display controller

CORE INTERFACES

The VF-111T core includes standard interfaces for host CPU access and video input. The VF-111T core includes a 32-bit, AMBA 4 Peripheral Bus (APB) slave interface. The APB provides low complexity transfers of configuration information to the core. All internal configuration and status registers are accessible from the APB.

Input image data is transferred via a streaming interface with industry standard flow control including separate syncs and data enable. Frame and line delimiter signals are supported with either 1 or 2 pixels per input clock cycle. Deep color is supported through the use of 48 bit pixel inputs. Other color depths are supported through selective use of these input ports.



PHY INTERFACE

The Trilinear VF-111T Link Controller interfaces to an external PHY which implements the gigabit transceivers necessary for the DisplayPort 1.4a standard. Several PHY implementations are currently available from Trilinear Technologies including 28nm, 40nm and 65nm. FPGA targeted implementations are also available. Please contact a sales representative for more information.

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the VF-111T transmitter core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

Trilinear Technologies has validated the core using the DisplayPort compliance test suite. The results of the compliance testing are available upon request. Extensive interoperability testing has also been conducted using a wide variety of shipping products.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

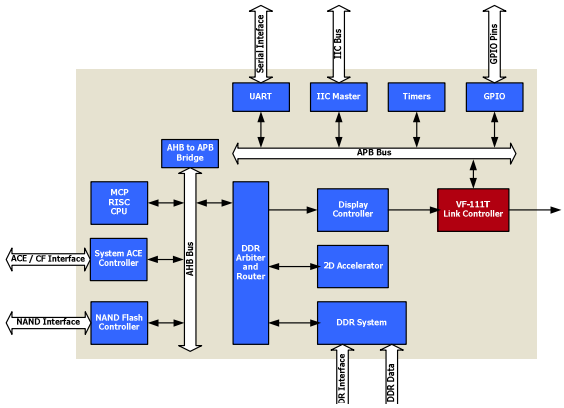
Trilinear Technologies delivers an extensive design database for the VF-111T link controller core. The database includes all the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver
- C Link Policy Maker

REFERENCE HARDWARE

The VF-111T core is available for demonstration and early software prototyping on the Trilinear “Cobra” development system. The Cobra development system is based on the Xilinx kc705 board and provides a high degree of functionality including a 32-bit MIPS processor capable of running custom applications.

Using the integrated SD Card system, custom application software can be loaded onto the system for early development. The video output system uses a standard daughter card which includes DisplayPort input and output connectors. The DisplayPort output can drive monitors up to and including 8K in resolution. Each Cobra system includes a host processor and peripheral suite running a flash based ROM monitor which loads at power up. The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The VF-111T Link Controller is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit MIPS processor
- Embedded ROM monitor
- Standard peripheral suite
- Internal AMBA bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-3 Memory System

- 512 MB minimum PC3-8500
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

DisplayPort Transmitter

- Driven from the internal timing controller
- Software policy maker
- 1,2, or 4 lanes
- 1.62Gbps, 2.7Gbps and 5.4Gbps

Onboard LCD Controller

- Programmable display timing controller
- Display path supports multiple color depths
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx kc705 Based System

- Xilinx Kintex-7 FPGA
- SD card mass storage
- DisplayPort transmitter and receiver

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