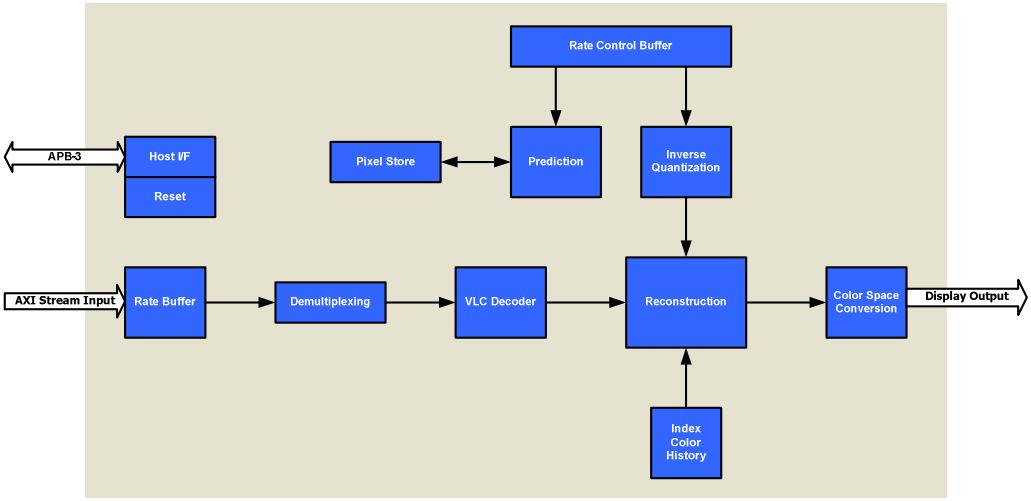
M25 Display Stream Compression (DSC 1.2) Decoder

The Display Stream Compression (DSC) standard from the Video Electronics Standards Association (VESA) offers visually lossless compression for high definition (HD) video in broadcast, automotive, medical and consumer electronics applications. The Trilinear Technologies M25 DSC 1.2 Decoder offers real time decompression of HD streams with resolutions from 480p up to 8K. The decoder core is fully compliant with the VESA DSC 1.2 standard and is available for both FPGA and ASIC platforms.

The M25 core is delivered with an industry standard AMBA 3.0 Peripheral Bus interface for host configuration and decoder control. The encoded input interface is AXI4-Stream Protocol compliant and the output interface uses a streaming data structure with associated line and frame formatting signals. The DSC 1.2 Decoder core supports 8, 10, 12, 14 or 16 bits per pixel using either the RGB or YCbCr in 4:4:4 or 4:2:2 format.

The M25 DSC 1.2 Decoder core ships with a complete 'C' reference driver and a fully documented API. The core is available on the Trilinear Technologies' Cobra Development platform based on the Xilinx Kintex-7 FPGA family. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- VESA DSC 1.2 Compliant
- Capable of decoding 4K video at 30fps in FPGA and ASIC
- Decode 8K video at 30fps in ASIC applications
- Low gate count implementation
- Low latency implementation

Decoder Details

- RGB or YCbCr encoded input
- 8, 10 or 12 bits per color
- 4:2:0 and 4:2:2 support
- AXI 4 Stream Input Interface
- AMBA 3.0 APB Host Interface

Reference Software

- Complete reference driver
- Stream decoder sample application
- C source code provided

FPGA Development Platform

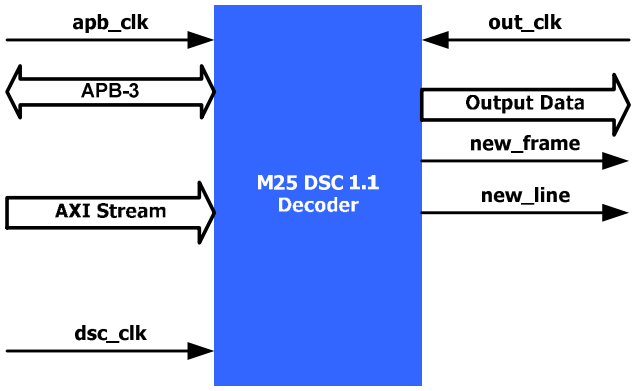
- 32-bit MIPS CPU based system
- HDMI Video Output
- Optional DisplayPort 1.3 output
- SD Card Stream Storage
- Hardware Driver and Reference Encoder Included

CORE INTERFACES

The M25 core implements industry standard interfaces for host CPU access, encoded data transfer and display data presentation. The core includes an AMBA 3.0 Peripheral Bus (APB) slave interface for programming and control. All internal configuration and status registers are accessible from the slave APB interface. An AXI 4 Stream interface is implemented to support the transfer of encoded data to the core at 2 bytes per clock cycle. The output interface uses a streaming interface with end of line and top of frame indicators.

The core implementation uses synchronous design techniques and a technology abstraction layer for internal SRAM buffers. This design methodology allows for the migration from FPGA or FPGA prototype to ASIC with no functional changes to the core. The decoder core is completely pipelined and can be stalled as necessary to properly manage input and output rates.

Three clock domains are implemented in the core. The stream and APB clocks are used to operate the applicable interfaces. The third domain provides an independent decoder clock that is used to run the core functions.



PERFORMANCE AND AREA

The implementation of the M25 core includes best in class design processes and is efficient in resource usage and operating frequency. 4K decode is performed using a core clock of 175MHz. In the TSMC 28HP process, the core requires less than 200K gates. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

VERIFICATION TESTING

Verification testing for the M25 Decoder core is fully compliant with VESA DSC 1.2 specification and has been validated using the VESA software model as the golden reference. Trilinear Technologies has completed extensive interoperability testing with 3rd party reference models and test suites. Interoperability testing has also been conducted on the reference hardware using a variety of shipping encoder products.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

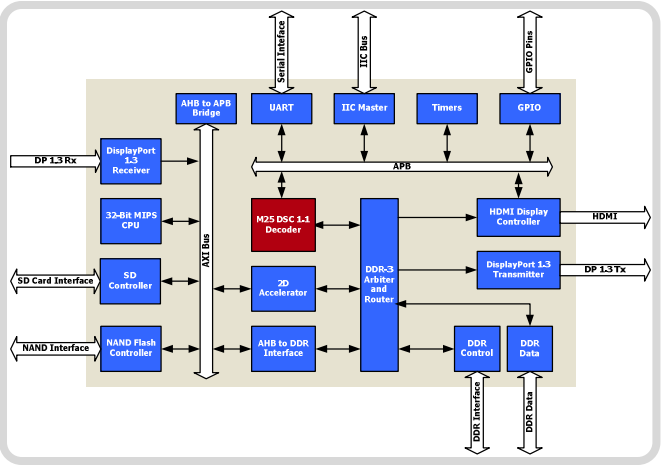
Trilinear Technologies delivers an extensive design database for the M25 core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver

REFERENCE HARDWARE

The M25 core is available for demonstration and validation on the Trilinear “Cobra” development system. The Cobra development system is based on the Xilinx kc705 board and provides a high degree of functionality including a 32-bit processor capable of running custom applications.

Using the integrated SD Card system, encoded streams may be copied from SD Card to memory using either customer developed software or the included DSC video decoder application. The DSC file format is fully supported. The display output system makes use of the on-board HDMI interface and requires no additional daughter cards. An optional daughter card for DisplayPort output is available upon request.



AVAILABILITY / ORDERING INFORMATION

The M25 DSC Decoder is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available either directly from Trilinear Technologies or through a qualified distribution partner under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit MIPS processor
- Embedded ROM monitor
- 150MHz operation
- Internal AMBA 3.0 bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-3 Memory System

- 512 MB Total Storage Supported
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard HDMI Interface / Display Controller

- Programmable display timing controller
- HDMI Output up to 1900x1200 (154MHz)
- Optional DisplayPort 1.3 Output to 4K

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx kc705 Based System

- Xilinx Kintex-7 XC7K325T-2FFG900C FPGA
- SD Card programming interface for rapid field updates

Built in Networking

- Integrated Trilinear Ethernet MAC core optimized for video streaming applications
- 10 / 100 / 1G operation
- Marvell Ethernet PHY

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