M11

SD/HD DV Video Decoder

The Trilinear Technologies M11 digital video decoder core provides standards compliant DV decoding using a high-performance and low gate count implementation. The fully synchronous core decodes 25Mbps, 50Mbs, and 100Mps DV streams recorded at either 50Hz or 60Hz. Using a complete hardware implementation, the M11 core is capable of operating with low CPU overhead while providing the highest quality results.

Overview

- Decodes all DV bit rates and formats
- Low CPU overhead
- Memory interface tolerant of high latencies ideal in a shared memory architecture
- Fully synchronous soft-core
- Comprehensive support plan
- Complete HW / SW verification suite

Core Details

- IEEE-1180 Compliant IDCT Engine
- Fully Synchronous Design
- AMBA 2.0 APB Target Command and Control Bus Interface
- 128-bit Memory DMA for maximum decode performance
- 256MB addressable memory range
- Source code fully portable between FPGA and ASIC with no modifications
- Decoding core operating frequency from 75MHz (SD) to 133MHz (HD)

Flexible Control Interface

- Low overhead mode for frame decoding
- Incremental decode mode when fine control is required.

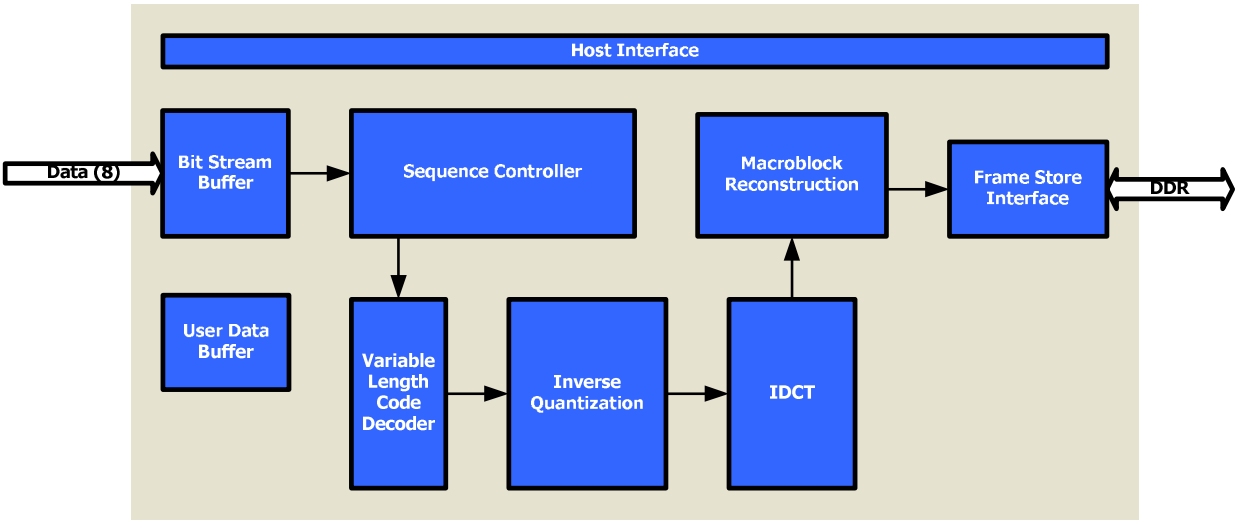
Reference Software

- Sample driver and video player application included in deliverables
- C source code provided
- Fully documented API

FPGA Development Platform

- Includes the M11 Video Decoder, DDR-3 interface, and display controller
- DVI digital output
- Integrated 32-bit microprocessor supports early software development

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The M11 accepts byte wide DV video streams from a dedicated input port. The input port uses bidirectional flow control handshaking for maximum flexibility and performance. The core is capable of operating in any mode independently of the host CPU so long as no bit stream errors are encountered. The host CPU has access to a full range of information and control parameters to modify the behavior of the decoding process to permit audio / video synchronization.

Bit Stream Buffer
The bit stream buffer holds small sections of the DV stream for maximum decode performance. The buffer reloads using a high speed, handshake enabled streaming mode. Byte streaming mode is supported through flow control signals and accepts bytes into the buffers without the overhead of bus transfers.

Sequence Controller
The Sequence Controller parses and dispatches each DIF block used in the decoding process. Video framing information is contained within the headers embedded in the stream and is provided to the entire decode pipeline. When video DIF blocks are detected, the Sequence Controller passes the bits in the stream to the Variable Length Code decoding or motion vector calculation.

Variable Length Code Decoder
Huffman encoded variable length codes representing IDCT run-level information are decoded in this block. IDCT run-level pairs are interpreted and decompressed before the IDCT data is forwarded to Inverse Quantization.

Inverse Quantization
The Inverse Quantizer applies the control information found in the input video stream to convert range compressed codes back into the DCT coefficients representing the residual data. This process includes the weight factors that are applied directly before the inverse DCT transform.

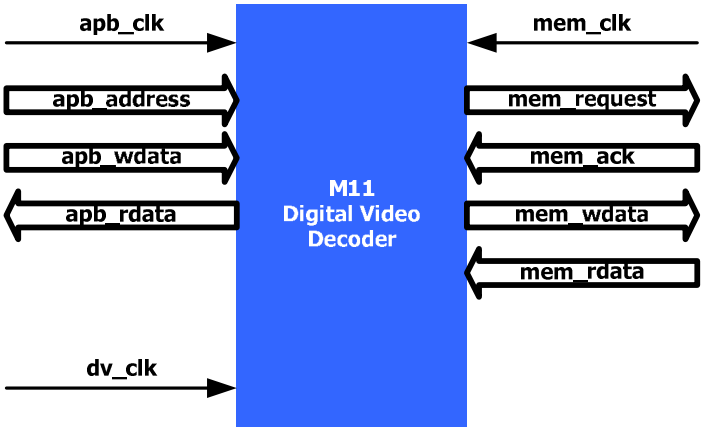
Inverse DCT
The inverse discrete cosine transform block is a high performance mathematical engine which transforms 8x8 blocks of picture data from the frequency domain back into the spatial domain. The IDCT engine maintains high throughput for the rapid decoding of picture samples.

Macroblock Reconstruction
Macroblock reconstruction consists of the proper ordering and compilation of the sample data from the IDCT engine. The resulting pixels are written to the Frame Store where they are then available for use in display or reference.

Frame Store Interface
The Frame Store is used to place decoded pictures into the memory subsystem. The interface uses a request-acknowledge flow control scheme suitable for implementation using a wide variety of memory technologies.

Host Interface
The host interface provides access to a wide range of information extracted from the input video source and provides additional capabilities. Important parameters from the video stream may be read from the M11 decoder and use by the host CPU for a variety of tasks including configuration of the display logic. The host interface also provides direct control of the decoding process and may be used to command the decoder to parse the input video stream in predetermined segments.

CORE INTERFACES



The M11 decoder core includes standard interfaces for host CPU access and frame store manipulation. Taking advantage of the modular nature of the design, Trilinear Technologies offers custom interfaces which conform to customer specifications. The modification of the interfaces requires no additional changes to the core decoding functions.

The standard M11 decoder core includes an AMBA 2.0 Peripheral Bus (APB). The APB provides low latency, low overhead transactions to the core. All internal configuration and status registers are accessible from the APB.

The frame store is accessed via a high speed DMA interface based on a split request / data protocol. The M11 core is capable of issuing multiple outstanding requests to the memory system which may be used for the optimization of transfers. Out of order retirement of memory requests is not supported. The frame store data paths are managed independently of the requests and consist of simple data and enable signals.

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the block level and completes with system level testing. With the M11 decoder core, module level testing consists of generating both randomized and corner case (boundary value) versions of all the fields. The VLC table decoder has been tested to pass every VLC table entry defined in the ISO and SMPTE standards. Testing of the IDCT unit is performed using a bit accurate model.

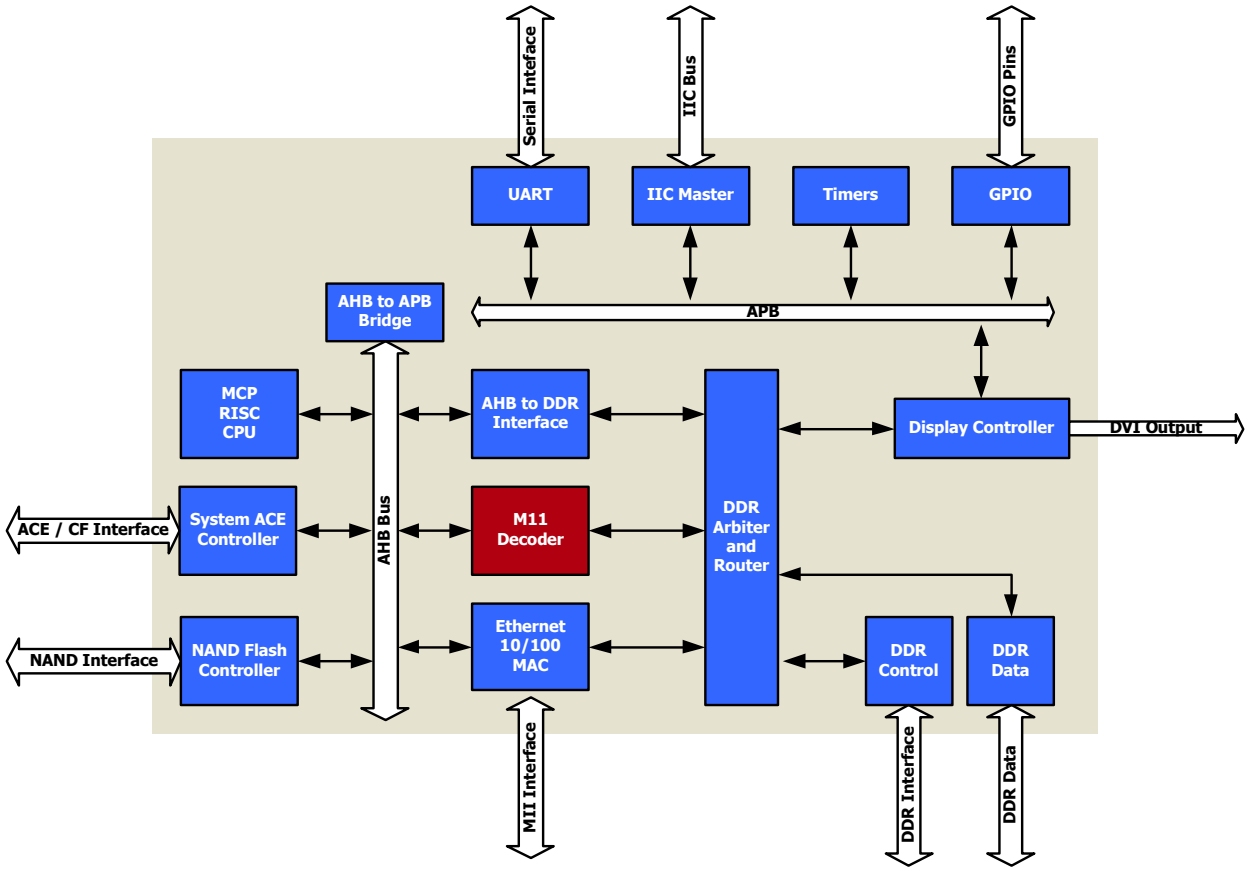
DESIGN DATABASE

Trilinear Technologies delivers the M11 Decoder Core with an extensive design database. The database includes all of the files required to implement the design on multiple platforms. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver
- C Reference video bit stream player application

REFERENCE HARDWARE

The M11 decoder core is available for demonstration and early software prototyping on the Trilinear "Vantage" development system. The Vantage development system is based on the Xilinx ml507 board and provides a high degree of functionality including an industry standard 32-bit microprocessor.



Using the integrated Compact Flash system, custom bit streams may be loaded into memory and decoded using either customer developed software or the included DV video player. The video output system makes use of the on-board DVI interface and requires no additional daughter cards.

Each Vantage system includes a host processor and peripheral suite running a flash based ROM monitor which loads at power up. The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.

Integrated Host Processor
- 32-bit RISC processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA 2.0 bus system

Built-In ROM Monitor
- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Ethernet
- Includes traditional shell commands

DDR-2 Memory System
- 256 MB PC4200
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard DVI Interface and LCD Controller
- Programmable display timing controller
- Display path supports multiple color depth

Support Functions
- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml505 Based System
- Xilinx Virtex-5 LX50T
- Compact Flash card programming interface for rapid field upgrades

Built in Networking
- Integrated Trilinear Ethernet MAC core optimized for video streaming applications
- 10 / 100 / 1G operation
- Marvell Ethernet PHY

AVAILABILITY AND ORDERING INFORMATION

The M11 DV Video Decoder is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the M11 or a version with customized interfaces. Custom host processor and DDR interfaces may be requested at no additional charge.

Please contact Trilinear Technologies for pricing and additional information.

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