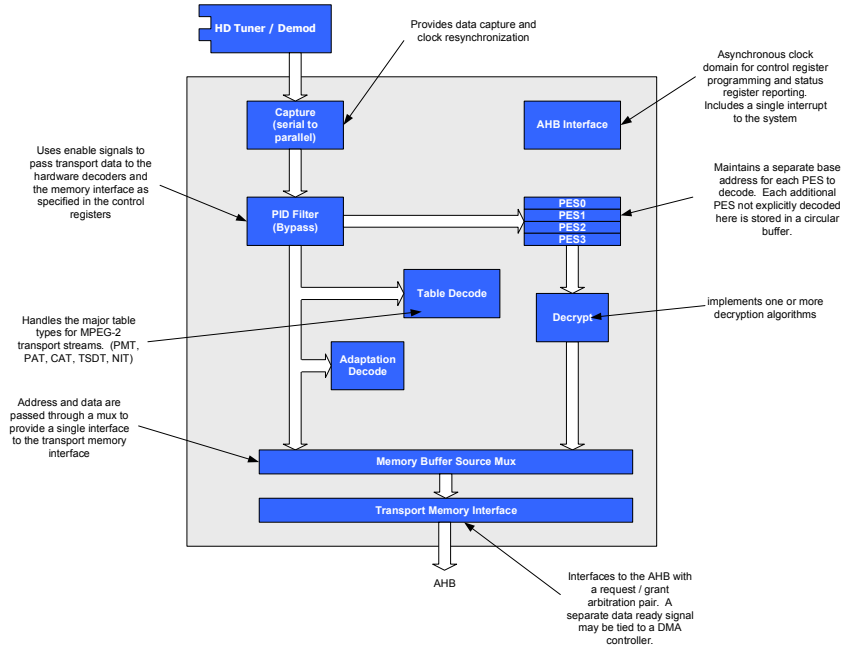
M107 MPEG-2 Transport Stream Decoder

The Trilinear Technologies M107 Transport Stream Decoder offers ISO13818-1 compliant transport stream decoding with performance and flexibility for a broad range of applications. With powerful packet ID and section filtering capabilities, the M107 processes serial or parallel bit streams at up to 150Mbits per second. The core is available with either an industry standard AMBA 2.0 High Speed Bus interface or an ABMA 3.0 AXI interface. Delivered as a flexible soft core, the M107 is available for ASIC and FPGA implementations using the same code base without the need for hand-crafted adaptation.

Worldwide data decryption is supported using optional modules for each standard. The M107 Decoder supports the TDES, DVB, AES, and Multi2 standards. Each of these standards may be optionally included in the core as required for the application.

The M107 TSD core ships with a complete 'C' reference driver and a fully documented API. The core is available on the Trilinear Technologies' Vantage Development platform based on the Xilinx Virtex5 FPGA family. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- ISO 13818-1 Compliant
- Supports DVB, ATSC, ARIB,OpenCable
- Integrated decryption support
- Supports FPGA and ASIC Implementations

Decode Details

- 32 PID Filters
- 32 section filters with 12 byte filter length
- 1-bit serial or 8-bit parallel input interface
- AMBA AHB or AXI
- System clock management

Integrated Decryption

- TDES with ECB, CBC, and CTS
- AES with ECB, OFB, CTR, CBC, and CFB
- DVB-CSA
- Multi2 with ECB, OFB, CBC, and CFB

Reference Software

- Complete reference driver
- Stream parser sample application
- C source code provided

FPGA Development Platform

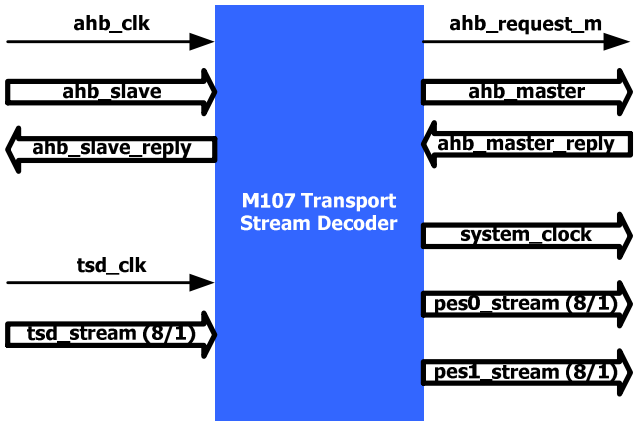
- 32-bit MIPS CPU based system
- DVI Video Output
- Downloadable Applications
- CompactFlash Stream Storage
- Hardware Driver and Reference Player Included

CORE INTERFACES

The M107 core includes standard interfaces for host CPU access and stream data transfer. The standard M107 core includes an AMBA 2.0 High Speed Bus (AHB) slave interface for programming and control. All internal configuration and status registers are accessible from the slave AHB interface. An AHB master interface is implemented to transfer decoded transport stream data to memory. AMBA 3.0 AXI interfaces are also available for the host slave and data master interfaces.

The core also supports two streaming bit or byte interfaces for PES data. These ports use a simplified ready/accept control handshake and may be connected directly to a digital video or audio decoder. The core is completely pipelined and can be stalled as necessary to properly manage input and output rates.

System clock management is performed using dedicated hardware output ports which can be used to feed an external clock management circuit. Clock drift is minimized through the proper timing of the management control signals in the transport data stream.



PERFORMANCE AND AREA

The M107 core implements best in class design processes and is very efficient in resource usage and clock rates. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

VERIFICATION TESTING

Verification testing of the M107 TSD core has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the M107 decoder core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of conditions.

The M107 TSD core is fully compliant with the ISO13818-1 specification as well as the applicable decryption standards. Trilinear Technologies has validated the core using external and internal compliance test suites. The results of the compliance testing are available upon request. Extensive interoperability testing has also been conducted using a wide variety of shipping demodulator products.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

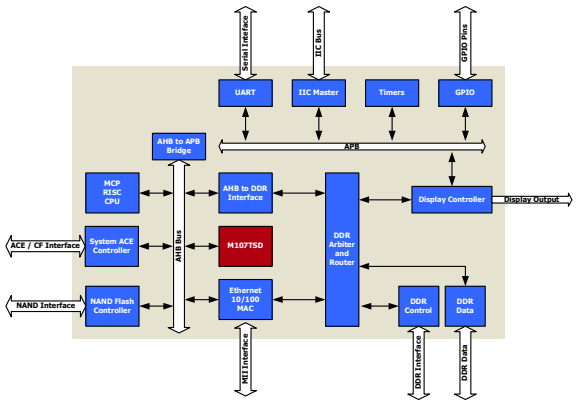
Trilinear Technologies delivers an extensive design database for the M107 core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver
- C Stream Parser Application

REFERENCE HARDWARE

The M107 core is available for demonstration and validation on the Trilinear “Vantage” development system. The Vantage development system is based on the Xilinx ml507 board and provides a high degree of functionality including a 32-bit processor capable of running custom applications.

Using the integrated Compact Flash system, transport streams may be loaded into memory and decoded using either customer developed software or the included MPEG-2 transport stream parser. The video output system makes use of the on-board DVI interface and requires no additional daughter cards. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The M107 MPEG-2 Transport Stream Decoder is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit RISC processor
- Embedded ROM monitor
- 150MHz operation
- Internal AMBA 2.0 bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-2 Memory System

- 256 MB PC4200
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard DVI Interface and LCD Controller

- Programmable display timing controller
- Display path supports multiple color depths
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml507 Based System

- Xilinx Virtex-5 LX70T
- Compact Flash card programming interface for rapid field updates

Built in Networking

- Integrated Trilinear Ethernet MAC core optimized for video streaming applications
- 10 / 100 / 1G operation
- Marvell Ethernet PHY

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