M4 H.264 Digital Video Decoder

The Trilinear Technologies M4 Digital Video Decoder is a hardware only implementation providing high quality and high performance h.264 video decoding. The M4 core supports the Constrained Baseline and Main Profiles as well as providing optional support for the High4:2:2 profile. All profiles are capable of decoding streams at the 4.2 level for FPGA implementations and the 5.1 level for ASIC implementations.

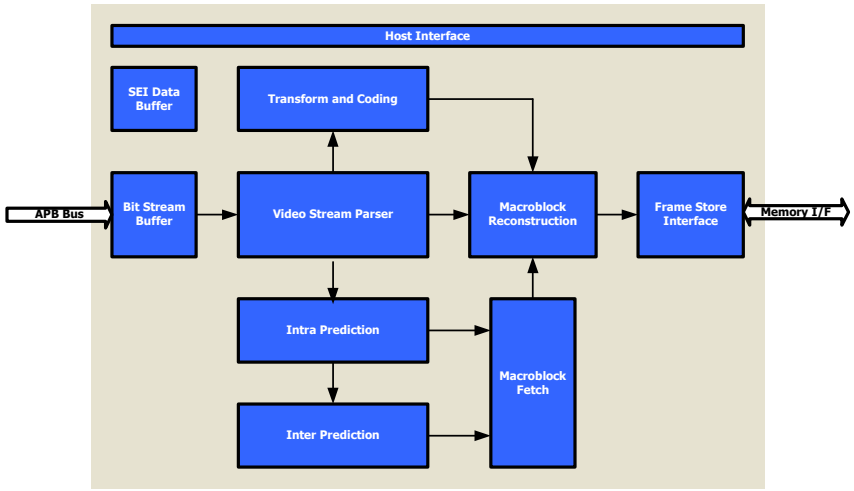
The host system communicates with the M4 core using the AMBA 3 APB slave interface. Control and status information provides real-time visibility of the core for applications requiring fine control of the decode process. For most applications, the core implements an autonomous mode where decoding proceeds without input from the host until a specified break point is reached.

The frame store is accessed through a direct high speed, wide bus, memory interface. Decoded picture storage can be configured based on the input video stream which allows the minimum amount of memory to be allocated for a specific stream. The memory system is tolerant of high latency which makes the M4 core ideal for implementation in a shared memory system.

The M4 Digital Video Decoder core ships with a complete reference driver and a fully documented API. The core is available on the Trilinear Technologies' Viper Development platform. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

The M4 core can be delivered as either a technology specific firm core or a technology independent soft core and may be implemented on both FPGA and ASIC platforms. The Trilinear Technologies' development process allows for the migration of soft cores from FPGA to ASIC for prototyping and production solutions with no core modifications.

BLOCK DIAGRAM



Overview

- Main and Baseline Profile
- Optional High 4:2:2 Profile
- Decodes up to level 4.2 (FPGA) or 5.1 (ASIC)
- Supports full performance FPGA and ASIC Implementations

Main Profile Support

- I, P, B-slices
- CAVLC and CABAC Entropy Coding
- In-Loop Deblocking Filter
- Interlaced Coding
- Multiple Reference Frames

High 4:2:2 Profile Support

- Transform Adaptivity
- Quantization Scaling Matrices
- Separate Cb/Cr QP Control
- 4:2:2 Color Space
- Monochrome Video Format

Core Details

- Low CPU Overhead
- Designed for a Shared Memory Architecture
- Low core clock rate <250MHz
- Up to 100Mb/sec @ 200MHz

FPGA Development Platform

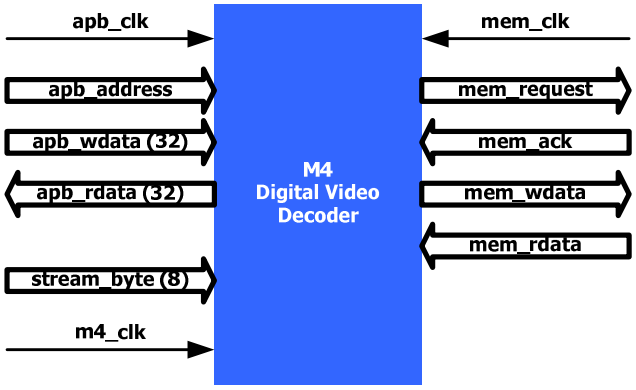
- 32-bit MIPS CPU based system
- DVI Video Output
- Downloadable Applications
- CompactFlash Stream Storage
- Hardware Driver and Reference Player Included

CORE INTERFACES

The M4 core includes a 32-bit, AMBA 3 Peripheral Bus (APB) slave interface. The APB provides low complexity transfers of configuration information to the core. All internal configuration and status registers are accessible from the APB.

Due to the modular architecture of the design, Trilinear Technologies is able to offer custom interfaces which conform to customer specifications. The modification of the interfaces requires no additional changes to the core processing functions. A sales representative can provide a list of currently supported interfaces.

The frame store is accessed via a high speed DMA interface based on a split request / data protocol. The M4 core is capable of issuing multiple outstanding requests to the memory system which may be used for the optimization of transfers. Out of order retirement of memory requests is not supported. The frame store data paths are managed independently of the requests and consist of simple data and enable signals.



PERFORMANCE AND AREA

The Trilinear M4 core utilizes best in class design practices and is very efficient in resource usage and operating rate. Resource usage and maximum clock rates for specific technology implementation are shown below. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

Technology	Fmax (MHz)	Area	SRAM	DSP
Xilinx Virtex6	150	9500 slices	26 BRAM	18
Lattice ECP4	150	TBD	TBD	TBD
Altera Stratix V	150	40K LE LUT	28 M9K	22
TSMC 90nm	150	360K gates	200K bits	
TSMC 65nm	150	385K gates	200K bits	

* Preliminary area estimates only

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the M4 decoder core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

Trilinear Technologies has validated the core using the h.264.1 Conformance Test Suite in addition to external and internal compliance test suites. The results of the compliance testing are available upon request. Extensive interoperability testing has also been conducted using a wide variety of shipping encoder products.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

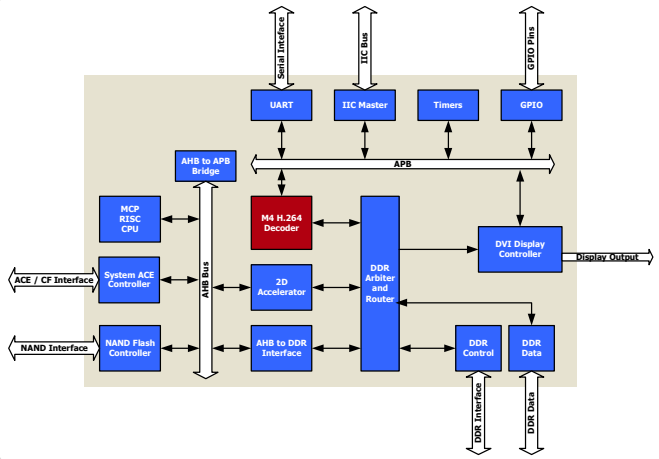
Trilinear Technologies delivers an extensive design database for the M4 core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver
- C Video Player Application

REFERENCE HARDWARE

The M4 H.264 Digital Video Decoder core is available for demonstration and early software prototyping on the Trilinear "Viper" development system. The Viper development system is based on the Xilinx ml605 board and provides a high degree of functionality including a 32-bit MIPS processor capable of running custom applications.

Using the integrated Compact Flash system, video bit streams may be loaded into memory and decoded using either customer developed software or the included H.264 video player. The video output system makes use of the on-board DVI interface and requires no additional daughter cards. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The M4 core is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit MIPS processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA 2.0 bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-3 Memory System

- 256 MB PC3-8500
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

DVI Transmitter

- Driven from the internal LCD controller
- Programmable display timing controller
- Display path supports multiple color depths
- Supports all SD / HD video modes
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml605 Based System

- Xilinx Virtex-6 LX240T
- Compact Flash card mass storage

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