

M2 MP@HL MPEG-2 Digital Video Decoder

The Trilinear Technologies M2 digital video decoder core is designed specifically for applications that demand high performance with uncompromising video quality. The fully synchronous M2 core is capable of decoding Main Profile @ High Level bit streams using a high speed direct to memory interface. The High Level is supported for the decoding of all profiles which include the 720p, 1080i, and 1080p formats with frame rates up to 120 Hz and compressed bit rates up to 125Mbits per second.

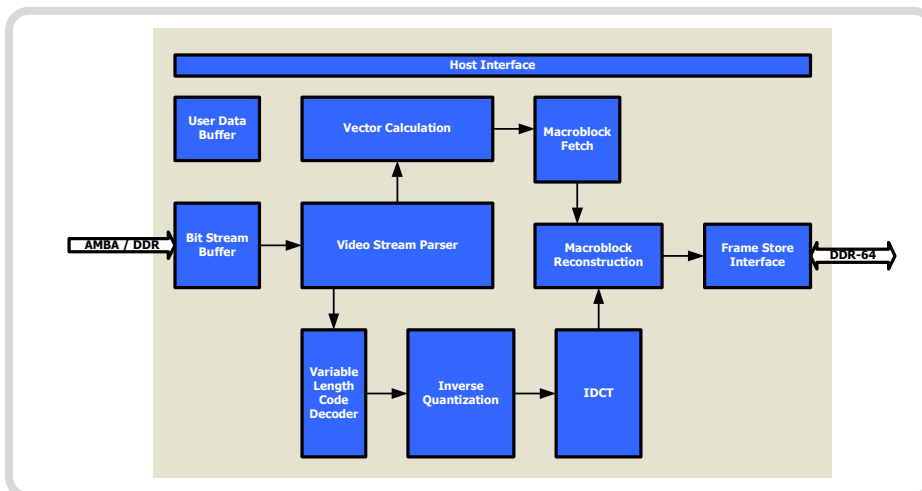
Compressed video streams are received through a flow control managed interface for maximum performance. Host system communication utilizes an industry standard AMBA APB or AHB slave interface. In most applications, the M2 core implements an autonomous decoding mode where operation proceeds without intervention from the host until a specified break point is reached. Control and status information provides real-time visibility for applications requiring fine control of the decode process.

An external frame store is accessed through a direct high speed, wide bus, memory interface designed for compatibility with most external DDR controllers. Decoded picture storage can be configured based on the input video stream which allows the minimum amount of memory to be allocated for a specific decode profile. The memory system is tolerant of high latency which is ideal for implementation in a shared memory system.

The M2 Digital Video Decoder core ships with a fully documented reference driver and a sample video player application. The core is available for demonstration on the Trilinear Technologies' Viper Development platform. This FPGA based reference system provides a complete environment for core evaluation as well as early software development.

The M2 core can be delivered as either a technology specific firm core or a technology independent soft core and may be implemented on both FPGA and ASIC platforms. The Trilinear Technologies' development process allows for the migration of soft cores from FPGA to ASIC for prototyping and production solutions with no core modifications.

BLOCK DIAGRAM



Overview

- Decodes up to Main Profile at High Level
- IEEE-1180 Compliant IDCT Engine
- Supports 4:2:2 and 4:2:0
- Capable of decoding a single HD stream or multiple SD streams
- Supports full performance FPGA and ASIC Implementations

Main Profile Support

- I, P, B-frames
- Interlaced Coding

High Level Profile Support

- Supports 1080p60 decode
- 4:2:2 Color Space
- 8, 9, 10 and 11 bit IntraDC precision

Core Details

- Low CPU Overhead
- Designed for a Shared Memory Architecture
- Multi-stream capable
- Low core clock rate
 - HD @ 135MHz
 - SD @ 65MHz
- Up to 120Mb/sec @ 150MHz

FPGA Development Platform

- 32-bit MIPS CPU based system
- DVI Video Output
- Downloadable Application Software
- CompactFlash Stream Storage
- Hardware Driver and Reference Player Included

FUNCTIONAL DESCRIPTION

The M2 is an efficient hardware implementation of an MPEG2 video decoder targeted for use in a broad range of applications. The M2 accepts video elementary streams from either the AMBA AHB slave port or can directly read the stream from memory. The core is capable of operating in any mode independently of the host CPU so long as no bit stream errors are encountered. The host CPU has access to a full range of information and control parameters to modify the behavior of the decoding process to permit audio / video synchronization and trick modes.

Video Stream Parser

The Video Stream Parser monitors the input video stream and extracts the relevant information for the decoding process. This information is contained within the hierarchical headers embedded in the stream and is provided to the entire decode pipeline. Selected user data may also be extracted from the input stream and placed in the local user data buffer for later retrieval by the host CPU. When slice information is detected, the video stream parser passes the bits in the stream to the appropriate function for either Variable Length Code decoding or motion vector calculation.

Variable Length Code Decoder

Huffman encoded variable length codes representing IDCT run-level information, motion vectors, and picture structure information are decoded in this block. IDCT run-level pairs are interpreted and decompressed before the IDCT data is forwarded to Inverse Quantization. Motion vectors and picture information are made available to the entire decoder.

Inverse Quantization

The Inverse Quantizer applies the control information found in the input video stream to convert range compressed codes back into the DCT coefficients representing the residual data. Custom inverse quantization tables as well as several scale factors are monitored as a part of this process.

Inverse DCT

The inverse discrete cosine transform block is a high performance mathematical engine which transforms 8x8 blocks of picture data from the frequency domain back into the spatial domain. The IDCT engine maintains high throughput for the rapid decoding of picture samples.

Vector Calculation

Motion vectors extracted from the input video stream are translated into row and column coordinates within the reference pictures by the Vector Calculation block. The vectors are modified according to a number of parameters found in the input stream headers including the motion compensation type used in the encoding process and the current picture type. The absolute coordinates of the predicted macroblock are passed to the Macroblock fetch unit for retrieval from the DDR picture store.

Macroblock Fetch

Using the coordinates determined in Vector Calculation, Macroblock Fetch issues the proper requests to the memory system to load the pixels into the decoder. In the case of multiple motion vectors, motion compensation predicted data is combined to form a single prediction.

Macroblock Reconstruction

Macroblock reconstruction consists of the combining of the motion compensated prediction data and the sample data from the IDCT engine. The resulting pixels are written to the Frame Store where they are then available for use in display or reference.

Frame Store Interface

The Frame Store is used for the storage of two reference pictures used during the decoding of the motion vectors for estimated pixels. In addition, the Frame Store contains two additional frames, the current decoded frame and the current display frame. The interface uses a request-acknowledge flow control scheme suitable for implementation using a wide variety of memory technologies.

Host Interface

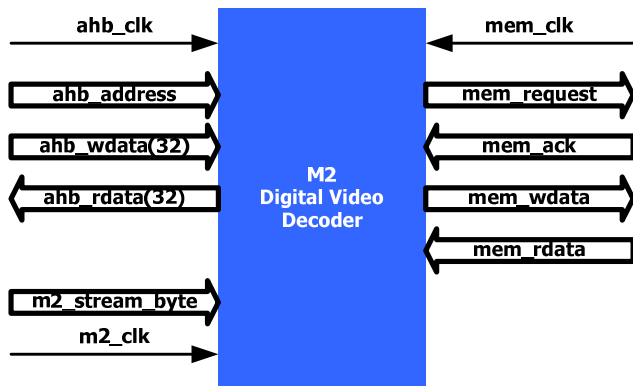
The host interface provides access to a wide range of information extracted from the input video source and provides additional capabilities. Important parameters from the video stream may be read from the M2 decoder and use by the host CPU for a variety of tasks including configuration of the display logic. The host interface also provides direct control of the decoding process and may be used to command the decoder to parse the input video stream in predetermined segments.

In lossy transmission environments or under other adverse conditions, errors in the input video stream may be detected in the decoding process. A simple interrupt controller within the host interface provides a level sensitive indicator. A status and mask register provide direct control over this capability.

CORE INTERFACES

The M2 decoder core includes standard interfaces for host CPU access and frame store manipulation. Taking advantage of the modular nature of the design, Trilinear Technologies offers custom interfaces which conform to customer specifications. The modification of the interfaces requires no additional changes to the core decoding functions.

The frame store is accessed via a high speed DMA interface based on a split request / data protocol. The M2 core is capable of issuing multiple outstanding requests to the memory system which may be used for the optimization of transfers. Out of order retirement of memory requests is not supported. The frame store data paths are managed independently of the requests and consist of simple data and enable signals.



PERFORMANCE AND AREA

The Trilinear M2 core utilizes best in class design practices and is very efficient in resource usage and operating rate. Resource usage and maximum clock rates for specific technology implementation are shown below. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

Technology	Fmax (MHz)	Area	SRAM	DSP
Xilinx Spartan6	135	6250 slices	14 BRAM	36
Xilinx Virtex6	135	6000 slices	14 BRAM	36
Altera Cyclone IV	135	32000 LE	16 M9K	42
Altera Stratix IV	135	26500 LE	16 M9K	42
TSMC 90nm	135	200K gates	76K bits	
TSMC 65nm	135	215K gates	76K bits	

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the M2 decoder core, module level testing consists of generating both randomized and corner case (boundary value) versions of all the headers, extensions and user data elements defined in ISO13818-2. The VLC table decoder has been tested to pass every VLC table entry defined in Appendix B. Testing of the IDCT unit if performed according to the IEEE-1180 conformance test, along with the additional tests called out in Annex A of ISO13818-2.

Motion compensated image reconstruction testing has been performed by generating randomized and corner case sets of the motion vector values in concert with the variable control parameters used to decode the vectors. Low level macroblock reconstruction has been verified to insure that the correct reference macroblocks are used properly under all motion compensation modes.

System level tests covered correct decoding of all streams in ISO13818-4 that are applicable to a MP@HL decoder.

DESIGN DATABASE

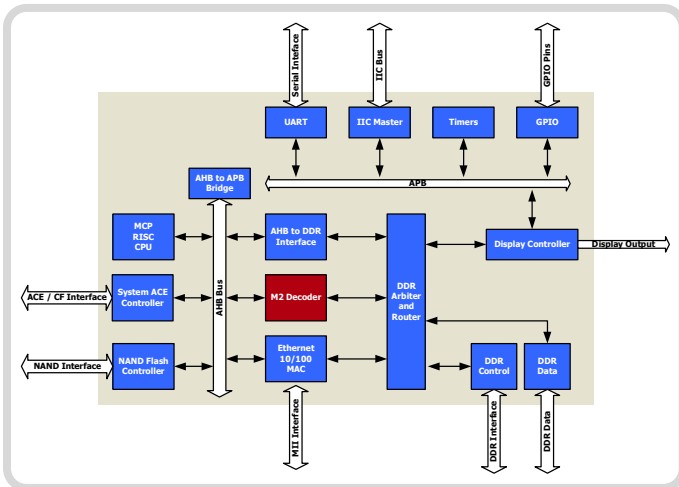
Trilinear Technologies delivers an extensive design database for the M2 decoder core. The database includes all of the files required to implement the design on multiple platforms. Reference software drivers and sample applications are included along with detailed documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- C Reference Driver and Player Application

REFERENCE HARDWARE

The M2 MPEG-2 Digital Video Decoder core is available for demonstration and early software prototyping on the Trilinear “Viper” development system. The Viper development system is based on the Xilinx ml605 board and provides a high degree of functionality including a 32-bit MIPS processor capable of running custom applications.

Using the integrated Compact Flash system, video bit streams may be loaded into memory and decoded using either customer developed software or the included MPEG-2 video player. The video output system makes use of the on-board DVI interface and requires no additional daughter cards. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The M2 core is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit MIPS processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA 3 bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-3 Memory System

- 256 MB PC3-8500
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

DVI Transmitter

- Driven from the internal LCD controller
- Programmable display timing controller
- Display path supports multiple color depths
- Supports all SD / HD video modes
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml605 Based System

- Xilinx Virtex-6 LX240T
- Compact Flash card mass storage

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