AVP-35 Content Adaptive Deinterlacer

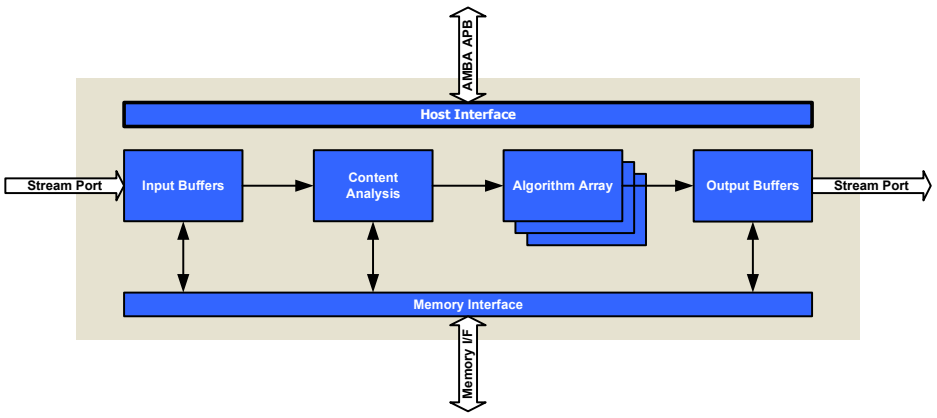
The Trilinear Technologies AVP-35 Content Adaptive Deinterlacer core provides advanced algorithms and high quality results for demanding video applications. The AVP-35 implements content adaptive processing in both the temporal and spatial domains. Temporal processing includes multiple level motion detection while spatial processing analyzes image details in order to enhance both large and small details. Additional non-linear filtering techniques further improve image quality.

At the heart of the AVP-35 core is a high precision motion detection unit which is capable of classifying movement between fields into multiple categories. These differing classes of motion are used by the reconstruction algorithms to provide the highest level of image quality possible. In addition to temporal analysis, the AVP-35 processing algorithms utilize spatial content analysis to further modify the progressive reconstruction process to preserve large and small image details. Additional non-linear processing algorithms are also applied during the reconstruction process resulting in high levels of image quality.

The AVP-35 is delivered as either a technology specific firm core or a technology independent soft core and may be implemented on both FPGA and ASIC platforms. The Trilinear Technologies' development process allows for the migration if soft cores from FPGA to ASIC for prototyping and production solutions with no core modifications. The AVP-35 core offers an optimal solution for both technologies without the typical limitations of performance in ASIC form and area in FPGA form. This flexibility is achieved through a state of the art internal architecture and best in class design practices.

The AVP-35 core ships with a comprehensive 'C' reference driver, a fully documented API and a sample video player application. The core is available for evaluation on the Trilinear Technologies' Viper Development platform. This FPGA based reference system provides a complete environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- Real time, content adaptive interlaced to progressive format conversion
- Zero CPU overhead after initial configuration
- Programmable reconstruction control from host

Core Details

- Core clock at 2x input clock
- Integrated cadence detection
- Multi-level motion detection
- Linear and non-linear filtering
- AMBA APB 3 Slave Interface
- 24, 30, 36-bit pixel support

Reference Software

- 'C' source code included
- Complete device driver
- Real time video player
- Fully documented API

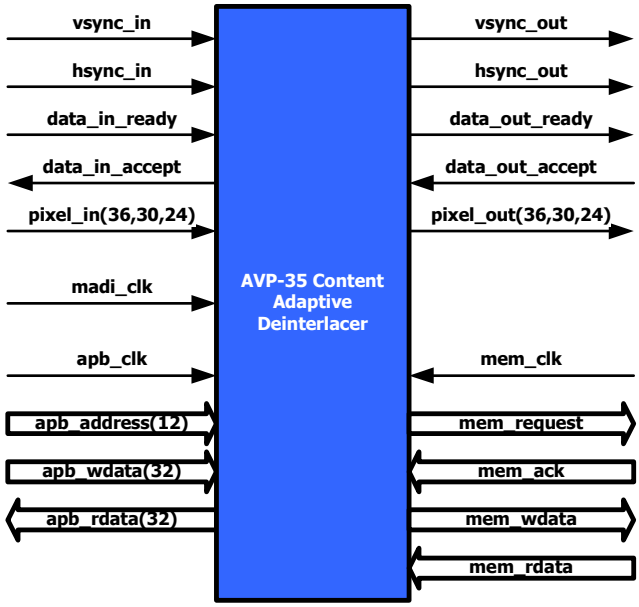
FPGA Development Platform

- 32-bit MCU based system
- Real time video input and output
- Includes the AVP-35 CA Deinterlacer, DDR memory system and display controller
- DVI digital output

CORE INTERFACES

The AVP-35 core utilizes an industry standard AMBA 3 Peripheral Bus (APB) slave interface. The APB provides low complexity access of configuration and status information. Taking advantage of the modular nature of the design, Trilinear Technologies offers the ability to customize the host processor interface to conform to customer specifications. The modification of the interfaces requires no additional changes to the core processing functions.

Input and output image data is transferred via a streaming interface with flow control or directly from memory. Flow control is managed via a ready/accept control signal pair which transfers a single pixel of image data when both are valid. The core is completely pipelined and can be stalled as necessary to properly manage input and output rates.



PERFORMANCE AND AREA

The Trilinear AVP-35 core has been implemented using best in class design practices for efficient resource usage and operating rate. Device resource usage and maximum clock rates for specific technology implementation are shown below. The clock rate listed is for the reconstruction of 1080p frames at 60Hz. Higher internal clock rates are possible for applications which require them. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

Technology	Fmax (MHz)	Area	SRAM	DSP
Xilinx Spartan6	150	3100 slices	20 BRAM	19
Altera Cyclone IV	150	15500 LE	20 M9K	19
Lattice ECP3	150	14000 LUT	20 MEM	19
TSMC 65nm	150	70K gates	200K bits	

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the AVP-35 core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

Trilinear Technologies provides a suite of processed images for the evaluation of the core. Customers may request the generation of additional images based on specific content. These images will be processed using internal models of the core and provided in jpeg or bitmap format.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

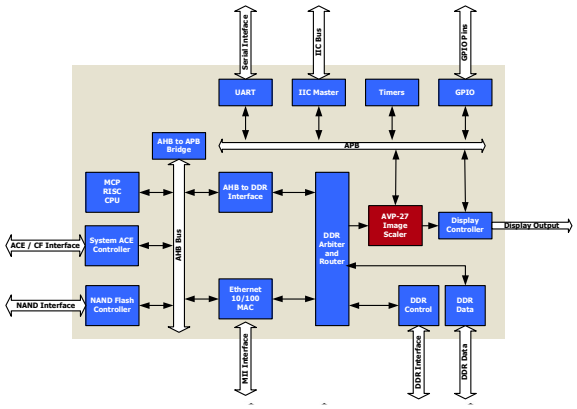
Trilinear Technologies delivers an extensive design database for the AVP-35 decoder core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver
- Sample video player application

REFERENCE HARDWARE

The AVP-37 core is available for demonstration and early software prototyping on the Trilinear “Vantage” development system. The Vantage development system is based on the Xilinx ml507 board and provides a high degree of functionality including a 32-bit processor capable of running custom applications.

Using the integrated Compact Flash system, custom application software can be loaded onto the system for early development. The video output system uses the on-board DVI interface and requires no additional daughter cards. The DVI output can drive monitors up to 1900x1200 in resolution. Each Vantage system includes a host processor and peripheral suite running a flash based ROM monitor which loads at power up. The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The AVP-35 Content Adaptive Deinterlacer is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit RISC processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-2 Memory System

- 256 MB PC4200
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard DVI Interface and LCD Controller

- Programmable display timing controller
- Display path supports multiple color depths
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml507 Based System

- Xilinx Virtex-5 LX70T
- Compact Flash card programming interface for rapid field updates

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