AVP-27 Frequency Domain Image Scaler

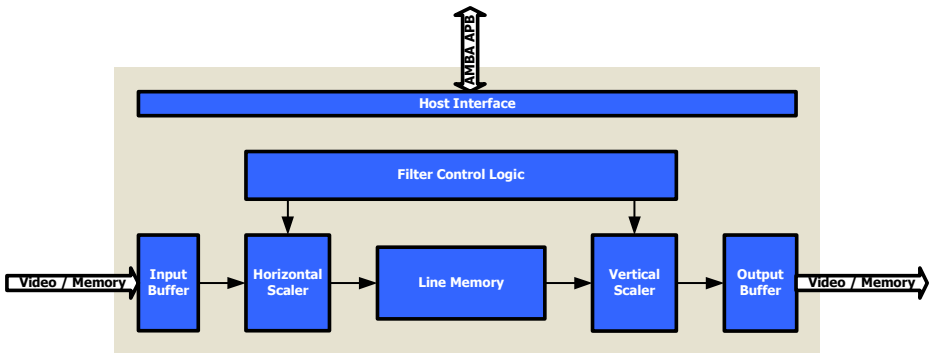
The Trilinear Technologies AVP-27 Image Scaler provides high quality results for demanding video applications. The AVP-27 balances complexity and resource usage for an optimal solution capable of generating images suitable for display in large screen applications. Host programmable scaler parameters allows the AVP-27 to be configured once on power up or reconfigured on the fly for input specific optimizations.

Using a multiple tap Finite Impulse Response (FIR) based algorithm provides high quality results using time tested frequency domain analysis of the scaling function. Developed in Matlab, the AVP-27 is provided with a complete range of filter settings including ultra-sharp and movie modes. Custom filters can be generated by customers and loaded into the core for testing. Additional non-linear processing elements may be enabled or disabled as needed.

The AVP-27 is delivered as either a technology specific firm core a technology independent soft core and may be implemented on both FPGA and ASIC platforms. The Trilinear Technologies' development process allows for the migration if soft cores from FPGA to ASIC for prototyping and production solutions with no core modifications. The AVP-27 core offers an optimal solution for both technologies without the typical limitations of performance in ASIC form and area in FPGA form. This flexibility is achieved through a state of the art internal architecture and best in class design practices.

The AVP-27 core ships with a complete 'C' reference driver and a fully documented API. The core is available on the Trilinear Technologies' Vantage Development platform. This FPGA based reference system provides a complete development environment for core evaluation as well as early software development.

BLOCK DIAGRAM



Overview

- Real time, frequency domain based image scaling
- Programmable coefficients
- Zero CPU overhead after initial configuration
- Variable scale factor with single pixel increments

Core Details

- Programmable coefficient memory for application specific adjustment
- 16X downscale
- 128X upscale
- AMBA APB-3 Slave Interface
- 24, 30, 36-bit pixel support

Reference Software

- 'C' source code included
- Complete device driver
- Real time video player
- Fully documented API

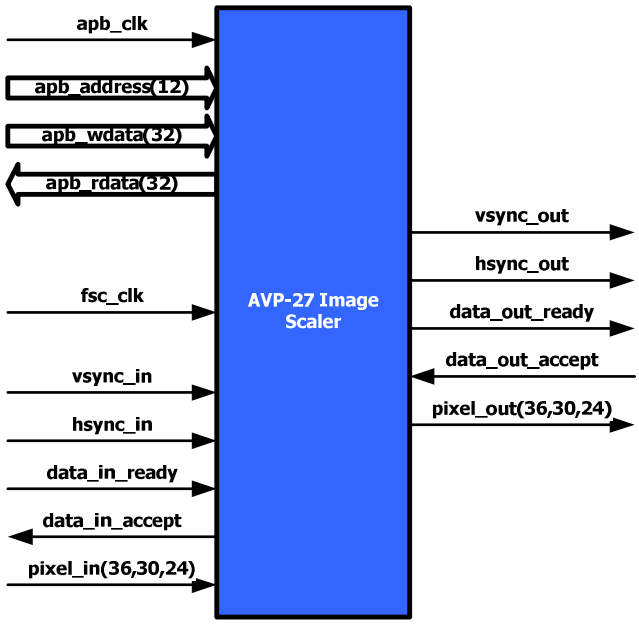
FPGA Development Platform

- 32-bit MCU based system
- Real time video input
- Includes the AVP-27 Image Scaler, DDR-2 system and display controller
- DVI digital output

CORE INTERFACES

The AVP-27 core includes standard interfaces for host CPU access and image data transfer. The standard AVP-27 core includes an AMBA 2.0 Peripheral Bus (APB) slave interface. The APB provides low complexity transfers of configuration information to the core. All internal configuration and status registers are accessible from the APB. Taking advantage of the modular nature of the design, Trilinear Technologies offers custom interfaces which conform to customer specifications. The modification of the interfaces requires no additional changes to the core processing functions.

Input and output image data is transferred via a streaming interface with flow control. Flow control is managed via a ready/accept control signal pair which transfers two pixels of image data when both are valid. The core is completely pipelined and can be stalled as necessary to properly manage input and output rates.



PERFORMANCE AND AREA

The AVP-27 core implements best in class design processes and is very efficient in resource usage and operating rate. Resource usage and maximum clock rates for specific technology implementation are shown below. For detailed information on area and timing, please contact Trilinear Technologies with the specific technology platform required.

Technology	Fmax (MHz)	Area	SRAM	DSP
Xilinx Spartan6	150	2400 slices	29 BRAM	14
Xilinx Virtex6	200	2200 slices	29 BRAM	14
Altera Cyclone IV	150	10500 LE	29 M9K	16
Altera Stratix IV	225	8500 ALUT	29 M9K	16
TSMC 90nm	275	75K gates	200K bits	
TSMC 65nm	350	85K gates	200K bits	

VERIFICATION TESTING

Verification testing has been performed using a bottom to top methodology. Testing is first performed at the module level and progresses up to system level testing. With the AVP-27 decoder core, module level testing consists of generating both randomized and corner case (boundary value) conditions across a wide variety of resolutions.

Trilinear Technologies provides a suite of scaled images for the evaluation of the core. Customers may request the generation of additional images based on specific content. These images will be processed using internal models of the core and provided as scaled bitmaps.

The core ships with a self-checking test bench intended to be used to illustrate the proper management of the input and output interfaces.

DESIGN DATABASE

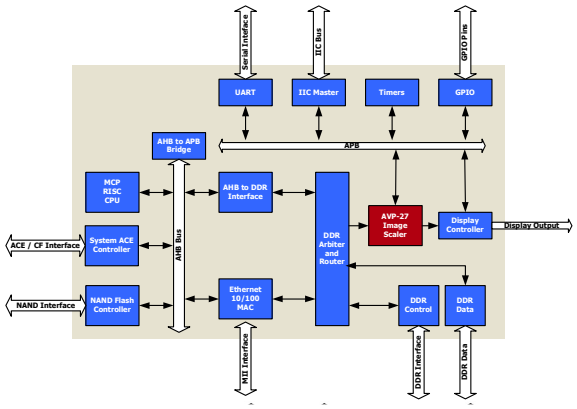
Trilinear Technologies delivers an extensive design database for the AVP-27 decoder core. The database includes all of the files required to implement the design on multiple platforms including FPGA and ASIC technologies. In addition to the core implementation files, reference software drivers and applications are included along with the associated documentation to reduce the amount of time for software development.

- HDL source files for the function design
- HDL source files for block level and top level testing
- Functional specification
- Timing constraints summary document
- Generic SRAM simulation models
- C Reference Driver

REFERENCE HARDWARE

The AVP-27 core is available for demonstration and early software prototyping on the Trilinear “Vantage” development system. The Vantage development system is based on the Xilinx ml507 board and provides a high degree of functionality including a 32-bit processor capable of running custom applications.

Using the integrated Compact Flash system, custom application software can be loaded onto the system for early development. The video output system uses the on-board DVI interface and requires no additional daughter cards. The DVI output can drive monitors up to 1900x1200 in resolution. Each Vantage system includes a host processor and peripheral suite running a flash based ROM monitor which loads at power up. The ROM monitor allows for the download of application code developed using the GCC tool chain. This capability allows for simultaneous hardware and software evaluation efforts.



AVAILABILITY / ORDERING INFORMATION

The AVP-27 Image Scaler is currently available as a soft core in one of several configurations. Customers may select from off-the-shelf versions of the core or a version with customized interfaces. Custom host processor and memory interfaces may be requested at no additional charge.

This product is available directly from Trilinear Technologies under several licensing models. Please contact Trilinear Technologies for pricing and additional information.

Integrated Host Processor

- 32-bit RISC processor
- Embedded ROM monitor
- Up to 150MHz operation
- Internal AMBA bus system

Built-In ROM Monitor

- Detects integrated IP at run time
- Applications built using GCC may be downloaded using the serial port or Compact Flash storage system
- Includes traditional shell commands

DDR-2 Memory System

- 256 MB PC4200
- 533 MHz Data Rate
- Peak bandwidth of 4.3 GB / sec

Onboard DVI Interface and LCD Controller

- Programmable display timing controller
- Display path supports multiple color depths
- Output up to 1900x1200 (154MHz)

Support Functions

- UART, Timers, GPIO
- Strata Flash Controller, 32 MB
- IIC Master

Xilinx ml507 Based System

- Xilinx Virtex-5 LX70T
- Compact Flash card programming interface for rapid field updates

Built in Networking

- Integrated Trilinear Ethernet MAC core optimized for video streaming applications
- 10 / 100 / 1G operation
- Marvell Ethernet PHY

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